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Optimizing Data Encoding Schemes to Reducing Energy Consumption in Network on Chip

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Abstract
The power dissipated by the links of a network-on-chip.the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces. we present a set of data encoding schemes to reduces the power dissipated by he links of an Network on chip. In proposed schemes are general and transparent with respect to the Network on chip (i.e., their application does not require any modification of the routers and architecture). We shows the both synthetic and real traffic scenarios of the effectiveness of the proposed schemes, which allow to save up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and less than 15% area overhead in network interface.

Keywords: Coupling switching activity, data encoding, interconnection on chip, low power network-on-chip, power analysis.

I. INTRODUCTION

SHIFTING from a silicon technology the results in faster and more power efficient gates but slow and more power hungry wires[1]. In this, more than 50% of the dynamic power is dissipated through interconnects in current processors, and this is expected to rise to 65%–80%of the next several years [2]. Global interconnect length does not suitable for smaller transistors and local wires. Chip size remains constant because the chip function continuously increase the RC delay and increases exponentially. At 32/28 nm, the RC delay in a 1-mm global wire at the minimum pitch is 25× higher than the intrinsic delay of a two-input NAND gate. If the raw computation the ability of instancing more and more cores in a single silicon die, it increasing the scalability issues, due to the efficient and reliable communication between increasing the no of cores is the real problem[3] the scalability and variability issues that characterize the ultra deep submicron meter era in Nowadays, the on-chip communication issues as relevant as, in some cases more relevant than, the computation-related issues [4]. In fact, the communication subsystem increases impacts in the traditional design objectives, including cost, area, performance, power dissipation, energy consumption, reliability, etc. As technology shrinks, the more significant fraction of the total power budget is complex in system-on-chip. In this paper, we focus on aimed to reducing the power dissipated by the network links. In fact, the power dissipated by the network links by routers and network interfaces and their contributions to increase the technology scale [5].we present a set of data encoding schemes operated at flit level on an end-to-end basis, which allows us to minimize the both switching activity and coupling switching activity of the routing path links and traversed by the packets. The proposed encoding schemes, which are transparent to the router implementation, are presented at both algorithmic level and the architectural level, and assessed by means of simulation and synthetic and real traffic scenarios. The analysis takes into account of several aspects of the design, including silicon area, power dissipation, and energy consumption. The results show that by using the proposed encoding schemes up to 51% of power and 14% of energy can be saved without any significant degradation in performance and with 15% area overhead in the Network interface.

II. RELATED WORKS AND CONTRIBUTIONS

In the next several years, the availability of chips with 1000cores is foreseen [6]. In these chips, total system power budget is dissipated by interconnection networks. The design of power-efficient interconnection networks has been focus of many works in the literature dealing with Network on chip architectures. These works concentrate on different components of the interconnection networks such as routers, NIs, and links. The data encoding scheme is another method it is to reduce the link power dissipation. The data encoding techniques may be classified into two categories. In the first category, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus

lines while ignoring the power dissipation owing to their coupling switching activity. In this category, we proposed the bus invert (BI) and INC- XOR have data patterns and graycode are used in encoding techniques. the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption. The works in the second category concentrate on reducing power dissipation through the reduction of the coupling switching [10], Among these schemes [10], the switching activity is reduced using many extra control lines. first the data both odd and even inverted number then transmission is performed using the kind of inversion which reduces more the switching activity. up to 39%. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching.

Time	Normal			Odd inverted		
	Type I			Types II,III,and IV		
t-1 t	00, 11 10, 01	00,11,01,10 01,10,00,11	01, 10 11, 00	00, 11 11, 00	00,11,01,10 00,11,01,10	01, 10 10, 01
	T1*	T1**	T1***	Type III	Type IV	Type V
t-1 t	Type II 01, 10 10, 01			Type I 01, 10 11, 00		
t-1 t	Type III 00, 11 11, 00			Type I 00, 11 10, 01		
t-1 t	Type IV 00,11,01,10 0011,01,10			Type I 00,11,01,10 01,10,00,11		

TABLE 1 EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION TYPES

The basic idea of the proposed approach is encoding the flits before they are injected into the network with is to minimizing the self-switching activity and the coupling switching activity traversed by the flits and self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer the end-to-end scheme. It takes advantage of the pipeline nature of the wormhole switching technique [4].for the proposed scheme, an encoder and a decoder block are added to the network interface.

III. OVERVIEW OF THE P ROPOSAL

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. This end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique [4].Note that since the same sequence of flits passes through all the links of the routing path, the encoding decision taken at the NI may provide the same power saving for all the links.For the proposed scheme, an encoder and a decoder block are added to the NI. Except for the header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link is minimized.

IV. ROPOSED ENCODING SCHEMES

The proposed encoding scheme is to reduce power dissipation by minimizing the coupling transition activities and interconnection network . The dynamic power dissipated by the interconnects and drivers is

$$P = [T_{0\to1}(C_S+C_l)+T_C C_C]V^2_{dd} F_{ck} \quad (1)$$

where $T_{0\to1}$ is the number of 0 transitions in the bus in two consecutive transmissions, T c is the number of correlated switching between physically adjacent lines, C s is the line to substrate capacitance, C l is the load capacitance, C is the coupling capacitance, Vdd is the supply voltage, and F ck is the clock frequency. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low. A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines does not change. The coupling transition activity, T c , is a weighted sum of different types of coupling transition contributions.Therefore

$$T_C = K_1T_1+K_2T_2+K_3T_3+K_4T_4 \quad (2)$$

Using (2), one may express (1) as

$$P = [T_{0\to1}(C_s+C_l)+(T_1+2T_2)C_c]v^2_{dd}F_{ck} \quad (3)$$

$$P\alpha T_{0\to1}C_s+(T_1+2T_2)C_c \quad (4)$$

we calculate the occurrence probability for different types of transitions. Consider that flit (t − 1) and flit (t) refer to the previous flit which was transferred the link in the flit respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur(Table I). the first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its (i +1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2,

and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability in Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively.

A scheme1

In scheme I, we focus on reducing the numbers of Type I transitions and Type II by converting in to type1. The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

$$P'\alpha T_{0\to1}+(K_1T_1'+K_2T_2'+K_3T_3'+K_4T_4')C_C \quad (5)$$

1) **Power Model**: If the flit is odd inverted dynamic power on the link in the self-transition activity, and the coupling transition before being transmitted, the activity of Types I, II, III, and IV, respectively. Table I reports. The first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its (i + 1)th line. For each partition, the first line represents the values at time t − 1 (t).

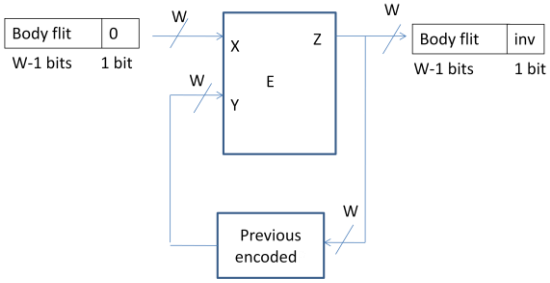


Fig.1.(a) encoder architecture scheme1 circuit diagram

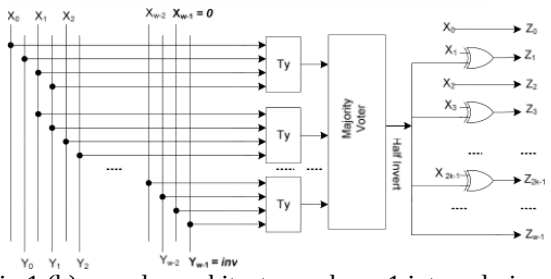


Fig.1.(b) encoder architecture scheme1 internal view of the encoder block(E)

$$T_{0\to1} = T_{0\to1(\text{odd})} + T_{0\to1(\text{even})} \quad (6)$$

$$\tfrac{1}{4}T_{0\to1}(\text{odd})+T_1+2T_2>\tfrac{1}{4}T_{0\to0}(\text{odd})+T_2+T_3+T_4+2T_1^{***} \quad (7)$$

We can approximate the exact condition as,

$$T_1+2T_2 > T_2+T_3+T_4+2T_1^{***} \quad (8)$$

the encoding scheme due to the error induced by the approximation but it simplifies the hardware implementation of encoder.

$$Ty = T_2+T_1-T_1^{***} \quad (9)$$

$$T_y > T_x \quad (10)$$

$$T_y+T_x = w-1 \quad (11)$$

$$Ty > \frac{(w-1)}{2} \quad (12)$$

Proposed Encoding Architecture:

The proposed encoding architecture, which is based on the odd invert condition defined by is shown in Fig. 1. We consider a link width of w bits. If no encoding is used. The w − 1 bits of the incoming (previous encoded) body flit are indicated by X i (Y i), i = 0,1,...,w − 2. The wth bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv= 0)

B. Scheme II

In the proposed encoding scheme II, we make use of both odd and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data of power reduction.

1)**Power model**: The odd inversion leads to power reduction when p'< p'' and p'< p. the power p'' is given by

$$P'' \alpha T_1+2T_4^{**} \quad (13)$$

$$T_2+T_3+T_4+2T_1^{***}<T_1+2T_4^{**} \quad (14)$$

$$2(T_2-T_4^{**}) <2T_y-w+1 \quad (15)$$

Based on (12) and (15), the odd inversion condition is obtained as

$$2(T_2-T_4^{**})<2T_y-w+1\ T_y>(w-1)/2 \quad (16)$$

$$T_2>T_4^{**} \quad (17)$$

$$2(T_2-T_4^{**})>2T_y-w+1\ T_2>T_4** \quad (18)$$

Proposed Encoding Architecture: The operating an encoder implementing the Scheme1in proposed encoding architecture, which is based on the odd invert condition of and the full invert condition of is shown in Fig. 2. Here again, the wth bit of the previously and the full invert condition of is shown in Fig. 2 In this encoder, in addition to the T y block in the Scheme I encoder, we have the T 2 and T ∗∗4 blocks which determine if the inversion based on the transition types T 2 and T ∗∗4 should be taken place for the link power reduction. The second stage is formed by a set of 1s blocks which count the number of 1s in their inputs.

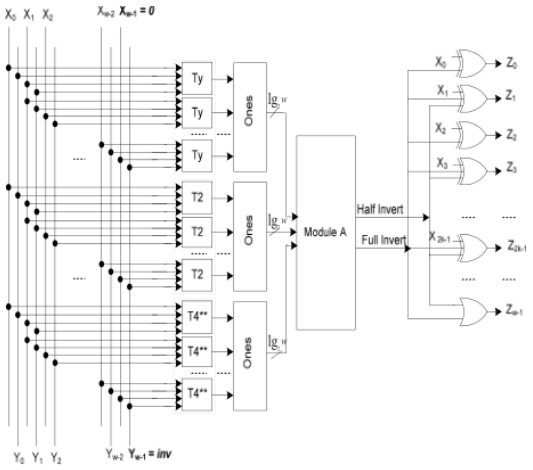


Fig.2.encoder architecture scheme11

The output of these blocks has the width of log 2 w. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction.

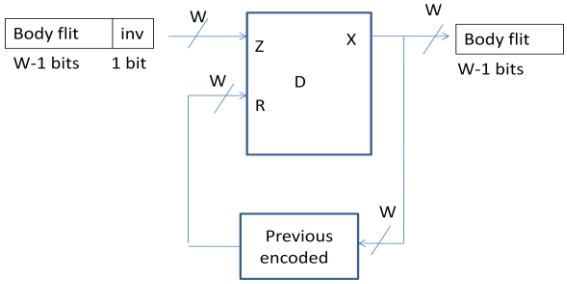


Fig.3.(a) decoder architecture scheme2 circuit diagram Fig.3.

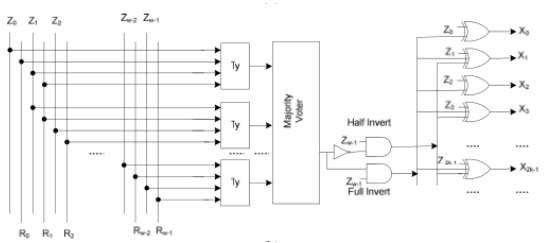


Fig.3.(b) decoder architecture scheme2 internal view of decoder block(D).

For this module, if is satisfied, the corresponding output signal will become "1." In case no invert action should be taken place, none of the output is set to "1." Module A can be implemented using full-adder and comparator blocks. The circuit diagram of the decoder is shown in Fig. 3.

C. Scheme III

In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type I (T ∗∗∗1) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as T ∗∗1/T ∗∗∗1 in the table are converted to Type IV/Type III transitions.

1)**Power model**: similar to the analysis given for scheme1,we approximate the condition p'''< p as

$$\mathbf{T_1+2T_2>T_2+T_3+T_4+2T_1^*} \quad \mathbf{(19)}$$

Defining

$$\mathbf{Te = T_2+T_1-T_1^*} \quad \mathbf{(20)}$$

Time	Normal			Even inverted		
	Type I			Types II,III,and IV		
t-1 t	01, 10 00, 11	00,11,01,10 10,01,11,00	00, 10 01, 10	01, 10 10, 01	00,11,01,10 00,11,01,10	00, 11 11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
t-1 t	Type II 01, 10 10, 01			Type I 01, 10 11, 00		
t-1 t	Type III 00, 11 11, 00			Type I 00, 11 01, 01		
t-1 t	Type IV 00,11,01,10 0011,01,10			Type I 00,11,01,10 10,01,11,00		

2) Proposed Encoding Architecture: The operating principles of this encoder are similar to those of the encoders implementing Schemes I and II. The proposed encoding architecture, which is based on the even invert condition .

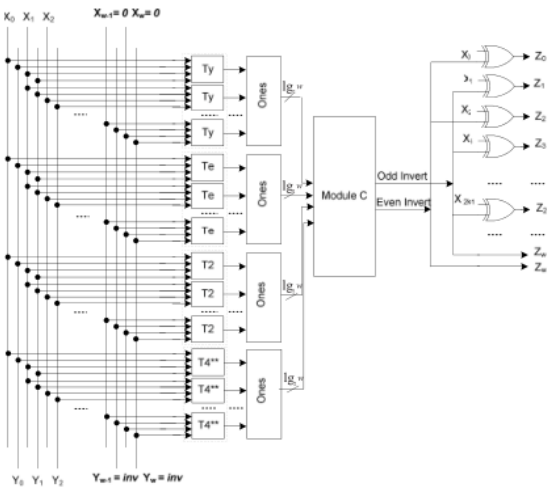


Fig.4 Encoder architecture scheme III.

In Fig.4 the first stage, we have added the T e blocks which determine if any of the transition types of T2,T ∗∗1, and T ∗∗∗1 is detected for each pair bits of their inputs. For these transition types, the even invert action yields link power reduction. Again, we have four Ones blocks to determine the number detected transitions for each. The output of the Ones blocks are inputs for Module C.

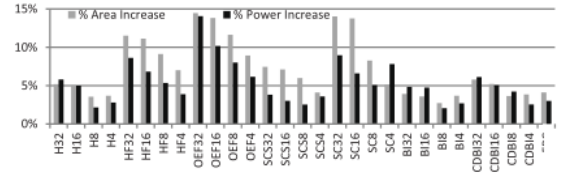


Fig.5. Percentage impact on silicon area and power dissipation of the network interface due to the data encoding/decoding logic

V. RESULTS AND DISCUSSION

The proposed data encoding schemes have been assessed by means of a cycle-accurate NOC simulator based on Noxim .The power estimation models of Noxim include NIs, routers and links. The NOC was clocked at 700 MHz while the baseline NI with minimum buffering and supporting open core protocol 2 and advanced high-performance bus protocol dissipated 5.3mW. The average power dissipated by the worm hole-based router was 5.7 mW. Based on a 65-nm UMC technology, a total capacitance of 592 fF/mm was assumed for an inter-router wire We assumed 2-mm 32-bit links and a packet size of 16 bytes (eight flits). We calculate the coupling capacitance of 0.237 and 0.947 nf, and we calculate the power (vdd = 0.9 V and F ck = 700 MHz).

The encoder and the decoder were designed in Verilog HDL described at the RTL level, synthesized with synopsys design compiler and mapped onto an UMC 65-nm technology library. the proposed encoding scheme I (H), scheme II (HF), and scheme III (OEF) are compared against SC and SCS [23], the BI coding the coupling driven BI (CDBI) coding and the forbidden pattern condition (FPC) codes.

B. Energy Analysis:

The proposed data encoding schemes in reducing the energy consumption,we consider an 8x8 mesh – based network on chip. We assumed a minimum of two-flit and maximum eight-flit packets, deterministic XY routing, and input FIFO buffers of four flits. Note that the coupling

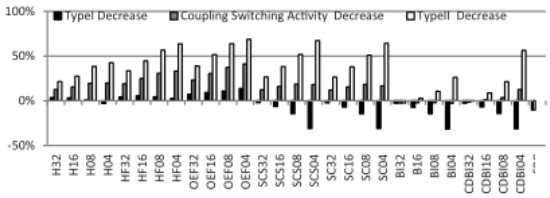


Fig. 6. Percentage of decrease Types I, II, and coupling switching activity obtained with different data encoding.

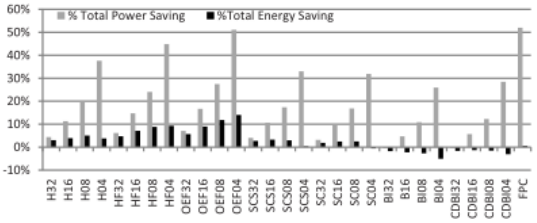


Fig. 7. Total power/energy saving using different data encoding schemes.

transition activity reduction is a weighted sum of the Types I and II transitions. To obtain the results for total power and energy saving shown in Fig. 7, we have considered all the interconnect Network on chip components including link, router, encoder, decoder, and NI. This part of Network on chip power/energy consumption constitutes an important fraction of the overall power/energy budget of the entire system. The results indicate that for a given partitioning of the link (4, 8, 16, or 32 bits), except for BI32 and CDBI32, all of the schemes provide us with some power savings. Among them, OEF4 and FPC shows the highest power savings.

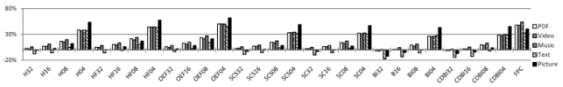


Fig. 8. Total power saving using different data encoding schemes for several data streams.

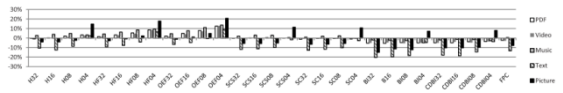


Fig. 9. Total energy saving using different data encoding schemes for several data streams.

It shows the highest power savings. This shows that our proposed schemes provide more power reductions when compared with other schemes. The power savings obtained when different data sets including PDF, video, music, text, and picture are used as the workloads are given in Fig. 8 (Fig. 9)it shows the energy savings for all the data streams considered in this paper. Also, in the case of OEF4, the saving is the largest among all the encoding schemes. For this encoding scheme, the maximum of

energy and power more than 20% and 60%, respectively, was achieved for the picture workload. Higher (lower) activities provide more (fewer) opportunities for the power saving by the proposed encoding schemes. For these applications, the proposed encoding schemes may provide lower power/energy savings. In these cases, one may apply the coding technique only to the bits with higher switching activities as has been performed for low-power memory addressing schemes.

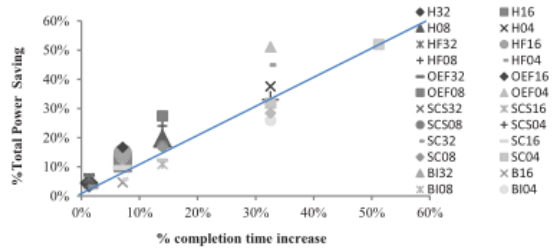
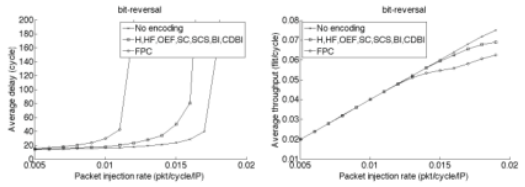


Fig. 10. Increase of the completion time versus increase of power dissipation.

C. Power Versus Performance

The tradeoff between the reduction of the average power dissipation of the communication system with the completion time is an important characteristic of the system. The percentage increase of completion time is defined as the percentage increase of the time needed to drain a given amount of traffic. In Fig. 10, this characteristic for each encoding scheme has been plotted. The points belonging to the lower (upper) region are characterized by a percentage of completion time increase which is greater (smaller) than the percentage of power dissipation reduction. From this graph, the OEF, HF, and H are the Pareto-optimal encoding schemes. We assume 32-bit links and packets of four flits (flit size is 32 bits). The schemes H, HF, OEF, SC, SCS, and BI require one, two, four, and eight additional bits (inv bits) when the link is divided into one, two, four,
and eight partitions, respectively. implementation outperforms H, HF, OEF, SC, SCS, and BI implementations by 13%. For both the average delay and the.



(a) (b)

Fig. 11. (a) Average delay. (b) Throughput using different data coding.

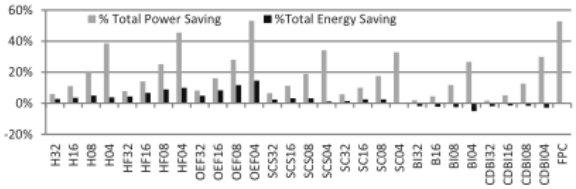


Fig.12.Total power/energy saving using different data encoding schemes.

D Multimedia System on Chip Case Study:

We analyze the efficacy of the proposed data encoding schemes on two complex heterogeneous systems. The first one, which is mapped to an 8 × 8 mesh, consisted of a triple video object plane decoder which has 38 core and multimedia and wireless communication which has 26 cores. We assumed a minimum of two-flit and maximum eight-flit packets, deterministic XY routing, and input FIFO buffers of four flits. The results of power and energy saving when different data encoding schemes have been presented in Fig.12. For these results, we assumed that the packet size was eight flits.

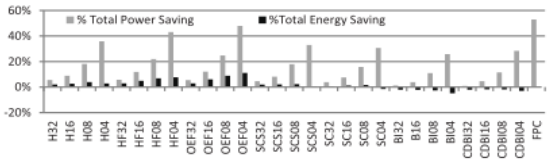


Fig. 13. Total power/energy saving using different data encoding schemes.

As can be observed from the results, the amount of power and energy reductions are similar to them results presented in Fig. 7. The second heterogeneous system consists of an MPEG-4 decoder, a picture-in-picture, a multi window display, a 263 encoder and mp3 decoder, and a 263 decoder and an mp3 decoder, which have a total of 58 cores . The system is mapped to an 8 × 8 mesh using the mapping technique described . As the results presented in Fig. 13 show, all of the schemes provide some power savings. Among them, FPC and OEF4 have the highest power savings. For the total energy consumption result, the highest reduction is 11% is achieved for OEF4. The amount of power and energy reductions for almost all the schemes are less than the corresponding results presented in Fig.12. This lowers the effectiveness of the data encoding techniques.

VI. CONCLUSION

We have presented a set of data encoding schemes aimed at reducing the power dissipated by the links of an NOC. In fact, the overall power dissipated by the communication system. As compared to the previous encoding schemes

proposed in the literature, the proposed schemes is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation in the deep sub micro meter technology.The proposed encoding schemes are agnostic to NOC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the Network Interface. It impacts the performance, power, and energy. The application of the proposed encoding schemes allows savings up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and less than 15% area overhead in the Network Interface.

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